WHAT IS CLAIMED IS:

1. A signal processing circuit comprising:

an analog integrated circuit having a first input terminal that receives a first-level analog signal during a first active period of a first switching signal and a second input terminal that receives a time varying reference signal, the first input terminal being coupled to a data line to receive a second-level analog signal corresponding to image charges of an image input element during a second active period of the first switching signal;

an inverter circuit that inverts and amplifies an output of said analog integrated circuit in response to an activated enable signal; and

an output circuit that generates a digital word indicative of a time period defined by a start signal and an end signal corresponding to a transition of an output of said inverter circuit,

wherein the enable signal is deactivated between an end point of the first active period and an end point of the second active period of the first switching signal.

2. The signal processing circuit of claim 1, wherein said inverter circuit comprises:

a first transistor having a first electrode coupled to a power supply voltage, a second electrode, and a gate coupled to the output of said analog integrated circuit;

a second transistor having a first electrode coupled to the second electrode of the first transistor, a second electrode, and a gate coupled to

the output of said analog integrated circuit; and

a third transistor having a first electrode coupled to the second electrode of the second transistor, a second electrode coupled to a ground voltage, and a gate coupled to the enable signal.

3. The signal processing circuit of claim 2, wherein the first transistor is a PMOS transistor, and the second and third transistors are NMOS transistors.

4. The signal processing circuit of claim 3, wherein the enable signal is active high.

5. The signal processing circuit of claim 1, wherein said inverter circuit comprises:

a first transistor having a first electrode coupled to a power supply voltage, a second electrode, and a gate coupled to the enable signal;

a second transistor having a first electrode coupled to the second electrode of the first transistor, a second electrode, and a gate coupled to the output of said analog integrated circuit; and

a third transistor having a first electrode coupled to the second electrode of the second transistor, a second electrode coupled to a ground voltage gate, and a gate coupled to the output of said analog integrated circuit.

6. The signal processing circuit of claim 5, wherein the first and

second transistors are PMOS transistors, and the third transistor is an NMOS transistor.

7. The signal processing circuit of claim 6, wherein the enable signal is active low.

8. The signal processing circuit of claim 1, wherein the time varying reference signal is a ramp signal varied with a predetermined inclination in response to the start signal.

9. The signal processing circuit of claim 1, wherein said analog integrated circuit comprises:

a first switch having a first terminal coupled to the first input terminal, and having a second terminal, the first switch being switchable responsive to the first switching signal;

a first capacitor having a first electrode coupled to the second terminal of the first switch, and having a second electrode coupled to an output terminal of said analog integrated circuit;

a second switch having a first terminal coupled to the second input terminal, and having a second terminal, the second switch being switchable responsive to a second switching signal; and

a second capacitor having a first electrode coupled to the second terminal of the second switch, and having a second electrode coupled to the output terminal of said analog integrated circuit.

10. A signal processing circuit comprising:

a sensor that provides a sensor signal at a sensor output terminal;

a sampling circuit having a first switch coupled between the sensor output terminal and a first electrode of a first capacitor, and a second switch coupled between a time varying reference signal and a first electrode of a second capacitor,

wherein second electrodes of the first and second capacitors are coupled to an output terminal of said sampling circuit, and wherein the first and second switches are respectively controlled by first and second switching signals;

an inverter circuit that inverts and amplifies a sampled signal provided at the output terminal of said sampling circuit, responsive to an activated enable signal; and

an output circuit that generates a digital word responsive to an output of said inverter circuit.

11. The signal processing circuit of claim 10, wherein the enable signal is deactivated at a timing in accordance with the first switching signal.

12. The signal processing circuit of claim 10, wherein said sensor provides a first-level analog signal as the sensor signal during a first active period of the first switching signal, and provides a second-level analog signal corresponding to sensor image charges as the sensor signal during a second active period of the first switching signal.

13. The signal processing circuit of claim 12, wherein the enable signal is deactivated between an end point of the first active period and an end point of the second active period.

14. The signal processing circuit of claim 10, wherein said inverter circuit comprises:

a first transistor having a first electrode coupled to a power supply voltage, a second electrode, and a gate coupled to the output terminal of said sampling circuit;

a second transistor having a first electrode coupled to the second electrode of the first transistor, a second electrode, and a gate coupled to the output terminal of said sampling circuit; and

a third transistor having a first electrode coupled to the second electrode of the second transistor, a second electrode coupled to a ground voltage, and a gate coupled to the enable signal.

15. The signal processing circuit of claim 14, wherein the first transistor is a PMOS transistor, and the second and third transistors are NMOS transistors.

16. The signal processing circuit of claim 15, wherein the enable signal is active high.

17. The signal processing circuit of claim 10, wherein said

inverter circuit comprises:

a first transistor having a first electrode coupled to a power supply voltage, a second electrode, and a gate coupled to the enable signal;

a second transistor having a first electrode coupled to the second electrode of the first transistor, a second electrode, and a gate coupled to the output terminal of said sampling circuit; and

a third transistor having a first electrode coupled to the second electrode of the second transistor, a second electrode coupled to a ground voltage, and a gate coupled to the output terminal of said sampling circuit.

18. The signal processing circuit of claim 17, wherein the first and second transistors are PMOS transistors, and the third transistor is an NMOS transistor.

19. The signal processing circuit of claim 18, wherein the enable signal is active low.

20. The signal processing circuit of claim 10, wherein the time varying reference signal is a ramp signal varied with a predetermined inclination.